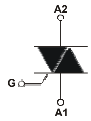
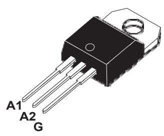
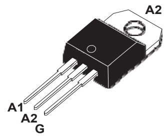
BTA24/BTB24

Features

- High current triac
- Low thermal resistance with clip bonding
- High commutation (4 quadrant) or very high commutation (3 quadrant) capability
- BTA series UL1557 certified
- Packages are RoHS (2002/95/EC) compliant







TO-220AB Insulated (BTA24) **TO-220AB (BTB24)**

Applications

Applications include the ON/OFF function in applications such as static relays, heating regulation, induction motor starting circuits, etc., or for phase control operation in light dimmers, motor speed controllers, and similar.

The snubberless versions (BTA/BTB...W series) are especially recommended for use on inductive loads, due to their high commutation performances. The BTA series provides an insulated tab (rated at 2500 V_{RMS}).

Description

Available either in through-hole or surface-mount packages, the **BTA/BTB24** triac series is suitable for general purpose mains power AC switching.

Table 1. Device summary

Symbol	Parameter	BTA24(1)	BTB24	Unit
$I_{T(RMS)}$	RMS on-state current	25	25	A
V_{DRM}/V_{RRM}	Repetitive peak off-state voltage	600 / 800	600 / 800	V
I_{GT} (Snubberless)	Triggering gate current	35 / 50	35 / 50	mA
I_{GT} (Standard)	Triggering gate current	-	50	mA

1. Insulated packages
2. 600 V version available only with I_{GT} = 50 mA (Snubberless and Standard)

TM: Snubberless is a trademark of STMicroelectronics

Characteristics

Table 2. Absolute maximum ratings

<table>
<tr><th>Symbol</th><th colspan="3">Parameter</th><th>Value</th><th>Unit</th></tr>
<tr><td rowspan="4">$I_{T(RMS)}$</td><td rowspan="4">RMS on-state current (full sine wave)</td><td>TOP3</td><td>T_c = 105°C</td><td rowspan="4">24</td><td rowspan="4">A</td></tr>
<tr><td>D2PAK
TO-220AB</td><td>T_c = 100°C</td></tr>
<tr><td>RD91 Ins
TOP3 Ins.</td><td>T_c = 100°C</td></tr>
<tr><td>TO-220AB Ins.</td><td>T_c = 75°C</td></tr>
<tr><td rowspan="2">I_{TSM}</td><td rowspan="2">Non repetitive surge peak on-state current (full cycle, T_j initial = 25°C)</td><td>F = 50 Hz</td><td>t = 20 ms</td><td>240</td><td rowspan="2">A</td></tr>
<tr><td>F = 60 Hz</td><td>t = 16.7 ms</td><td>260</td></tr>
<tr><td>I^2t</td><td>I^2t Value for fusing</td><td colspan="2">t_p = 10 ms</td><td>340</td><td>A^2s</td></tr>
<tr><td>dI/dt</td><td>Critical rate of rise of on-state current I_G = 2 x I_{GT} , $t_r \leq$ 100 ns</td><td>F = 120 Hz</td><td>T_j = 125°C</td><td>50</td><td>A/µs</td></tr>
<tr><td>V_{DSM}/V_{RSM}</td><td>Non repetitive surge peak off-state voltage</td><td>t_p = 10 ms</td><td>T_j = 25°C</td><td>V_{DRM}/V_{RRM} + 100</td><td>V</td></tr>
<tr><td>I_{GM}</td><td>Peak gate current</td><td>t_p = 20 µs</td><td>T_j = 125°C</td><td>4</td><td>A</td></tr>
<tr><td>$P_{G(AV)}$</td><td colspan="2">Average gate power dissipation</td><td>T_j = 125°C</td><td>1</td><td>W</td></tr>
<tr><td>T_{stg}
T_j</td><td colspan="3">Storage junction temperature range Operating junction temperature range</td><td>- 40 to + 150
- 40 to + 125</td><td>°C</td></tr>
</table>

Table 3. Electrical characteristics (T_j = 25°C, unless otherwise specified), Snubberless and logic level (3 quadrants) T25, BTA/BTB24...W

<table>
<tr><th rowspan="2">Symbol</th><th rowspan="2">Test Conditions</th><th rowspan="2">Quadrant</th><th rowspan="2"></th><th colspan="3">BTA/BTB</th><th rowspan="2">Unit</th></tr>
<tr><th colspan="2">CW</th><th>BW</th></tr>
<tr><td>I_{GT}(1)</td><td rowspan="2">V_D = 12 V R_L = 33Ω</td><td>I - II - III</td><td>MAX.</td><td colspan="2">35</td><td>50</td><td>mA</td></tr>
<tr><td>V_{GT}</td><td>I - II - III</td><td>MAX.</td><td colspan="3">1.3</td><td>V</td></tr>
<tr><td>V_{GD}</td><td>VD = VDRM RL = 3.3kΩ Tj=125°C</td><td>I - II - III</td><td>MIN.</td><td colspan="3">0.2</td><td>V</td></tr>
<tr><td>I_H(2)</td><td colspan="2">I_T = 500 mA</td><td>MAX.</td><td>50</td><td>50</td><td>75</td><td>mA</td></tr>
<tr><td rowspan="2">I_L</td><td rowspan="2">I_G = 1.2 I_{GT}</td><td>I - III</td><td rowspan="2">MAX.</td><td>70</td><td>70</td><td>80</td><td rowspan="2">mA</td></tr>
<tr><td>II</td><td>80</td><td>80</td><td>100</td></tr>
<tr><td>dV/dt (2)</td><td>V_D = 67 %V_{DRM} gate open</td><td>T_j = 125°C</td><td>MIN.</td><td>500</td><td>500</td><td>1000</td><td>V/µs</td></tr>
<tr><td>(dI/dt)c (2)</td><td>Without snubber</td><td>T_j = 125°C</td><td>MIN.</td><td>13</td><td>13</td><td>22</td><td>A/ms</td></tr>
</table>

1. Minimum I_{GT} is guaranteed at 5% of I_{GT} max.
2. For both polarities of A2 referenced to A1.

Table 4. Electrical characteristics (T_j = 25°C, unless otherwise specified), standard (4 quadrants), BTB24...B

Symbol	Test Conditions	Quadrant		Value	Unit
I_{GT} (1)	V_D = 12 V R_L = 33Ω	I - II - III	MAX.	50	mA
		IV		100	
V_{GT}		ALL	MAX.	1.3	V
V_{GD}	V_D = V_{DRM} R_L = 3.3 kΩ T_j = 125°C	ALL	MIN.	0.2	V
I_H (2)	I_T = 500 mA		MAX.	80	mA
I_L	I_G = 1.2 I_{GT}	I - III - IV	MAX.	70	mA
		II		160	
dV/dt (2)	V_D = 67 %V_{DRM} gate open	T_j = 125°C	MIN.	500	V/µs
(dV/dt)c (2)	(dI/dt)c = 13.3 A/ms	T_j = 125°C	MIN.	10	V/µs

1. Minimum I_{GT} is guaranteed at 5% of I_{GT} max.
2. For both polarities of A2 referenced to A1.

Table 5. Static characteristics

Symbol	Test Conditions			Value	Unit
V_{TM} (1)	I_{TM} =35 A t_p = 380 µs	T_j = 25°C	MAX.	1.55	V
V_{t0} (1)	Threshold voltage	T_j = 125°C	MAX.	0.85	V
R_d (1)	Dynamic resistance	T_j = 125°C	MAX.	16	m
I_{DRM} I_{RRM}	V_{DRM} = V_{RRM}	T_j = 25°C	MAX.	5	µA
		T_j = 125°C		3	mA

1. For both polarities of A2 referenced to A1.

Table 6. Thermal resistance

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Junction to case (AC)	TO-220AB	0.8	°C/W
		TO-220AB Insulated	1.7	
$R_{th(j-a)}$	(1)S = 1 cm² Junction to ambient	TO-220AB / TO-220AB Insulated	50 60	°C/W

1. S = Copper surface under tab.

Figure 1. Maximum power dissipation versus RMS on-state current (full cycle)

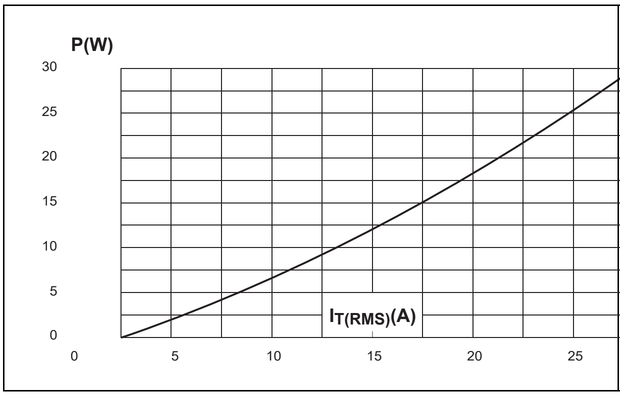


Figure 2. RMS on-state current versus case temperature (full cycle)

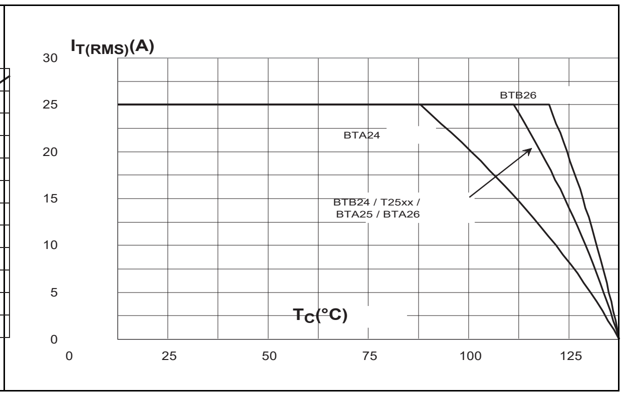


Figure 3. D^2PAK RMS on-state current versus ambient temperature (printed circuit board FR4, copper thickness: 35µm) (full cycle)

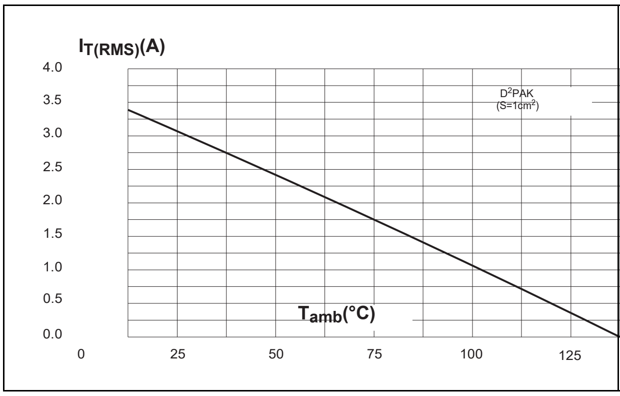


Figure 4. Relative variation of thermal impedance versus pulse duration

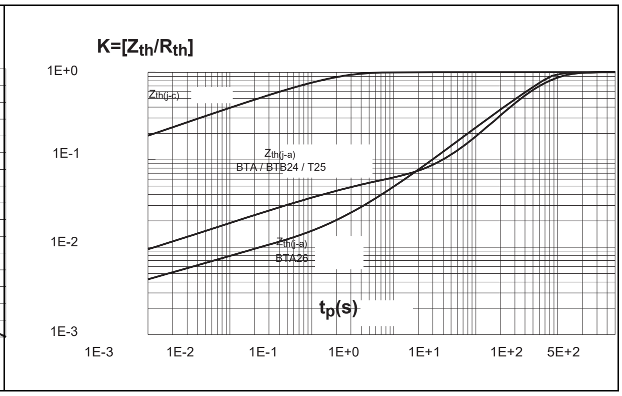


Figure 5. On-state characteristics (maximum values)

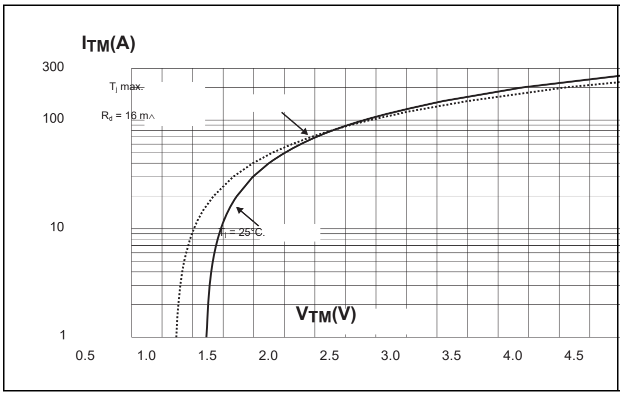


Figure 6. Surge peak on-state current versus number of cycles

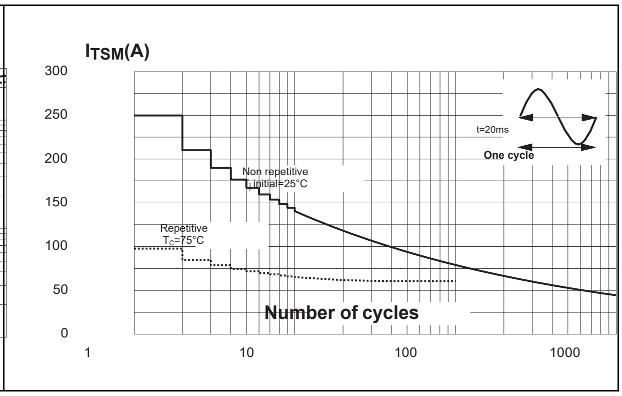


Figure 7. Non-repetitive surge peak on-state current for a sinusoidal pulse with width t_p < 10 ms and corresponding value of I^2t

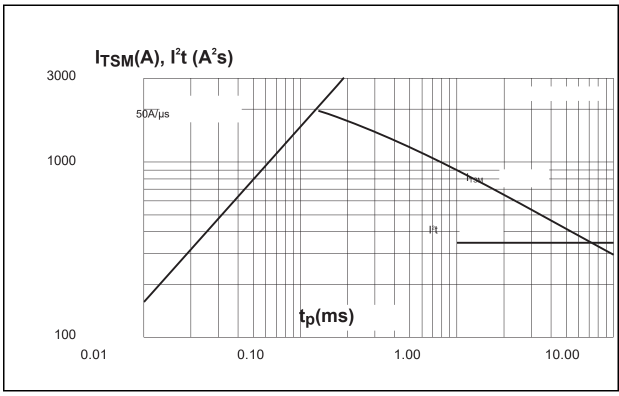


Figure 8. Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values)

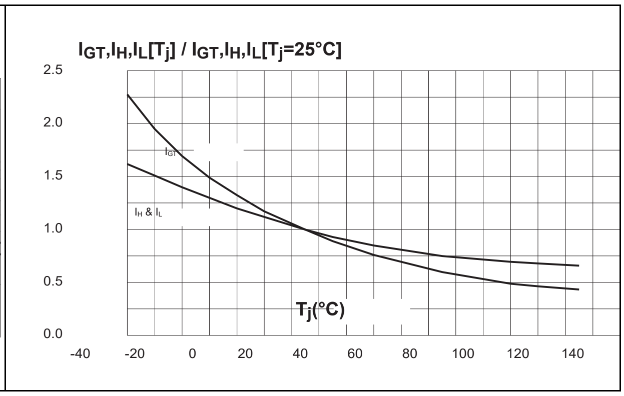


Figure 9. Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values)

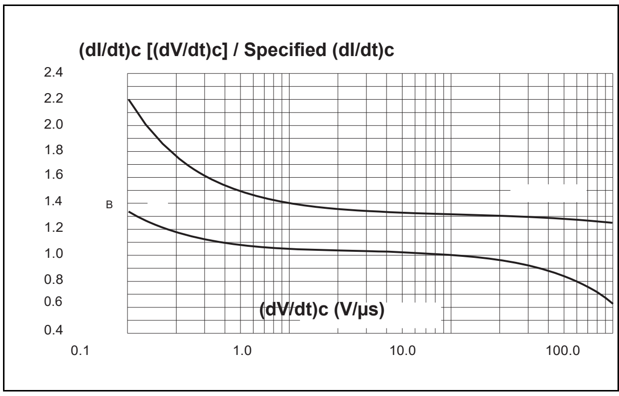


Figure 10. Relative variation of critical rate of decrease of main current versus T_j

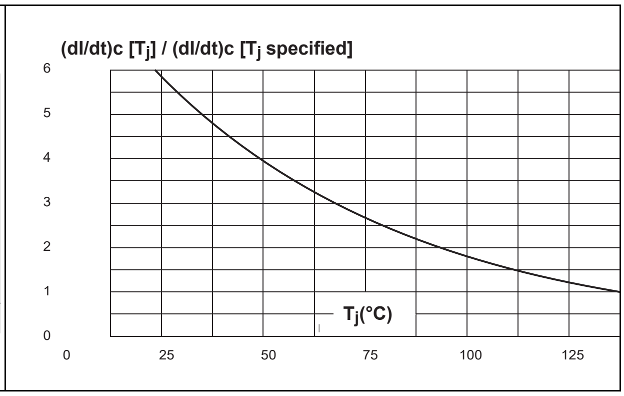


Figure 11. D²PAK thermal resistance junction to ambient versus copper surface under tab (printed circuit board FR4, copper thickness: 35 µm)