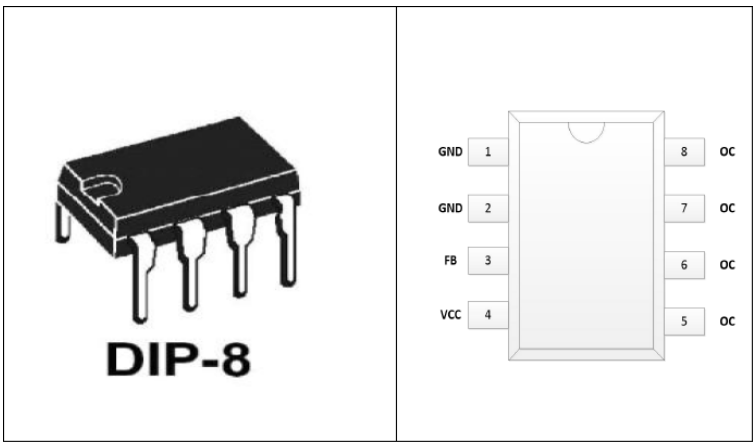
## Features

- Wide Voltage Input 85-265$V_{AC}$
- Switching frequency 65KHz
- Built-in 700V MOSFET
- Built-in self-powered circuit
- Frequency-hopping mode
- Built-in slope compensation
- Low standby consumption <270mW@230$V_{AC}$
- Rich protection: OLP,OCP,OTP,UVLO
- Power capability ⩽24W



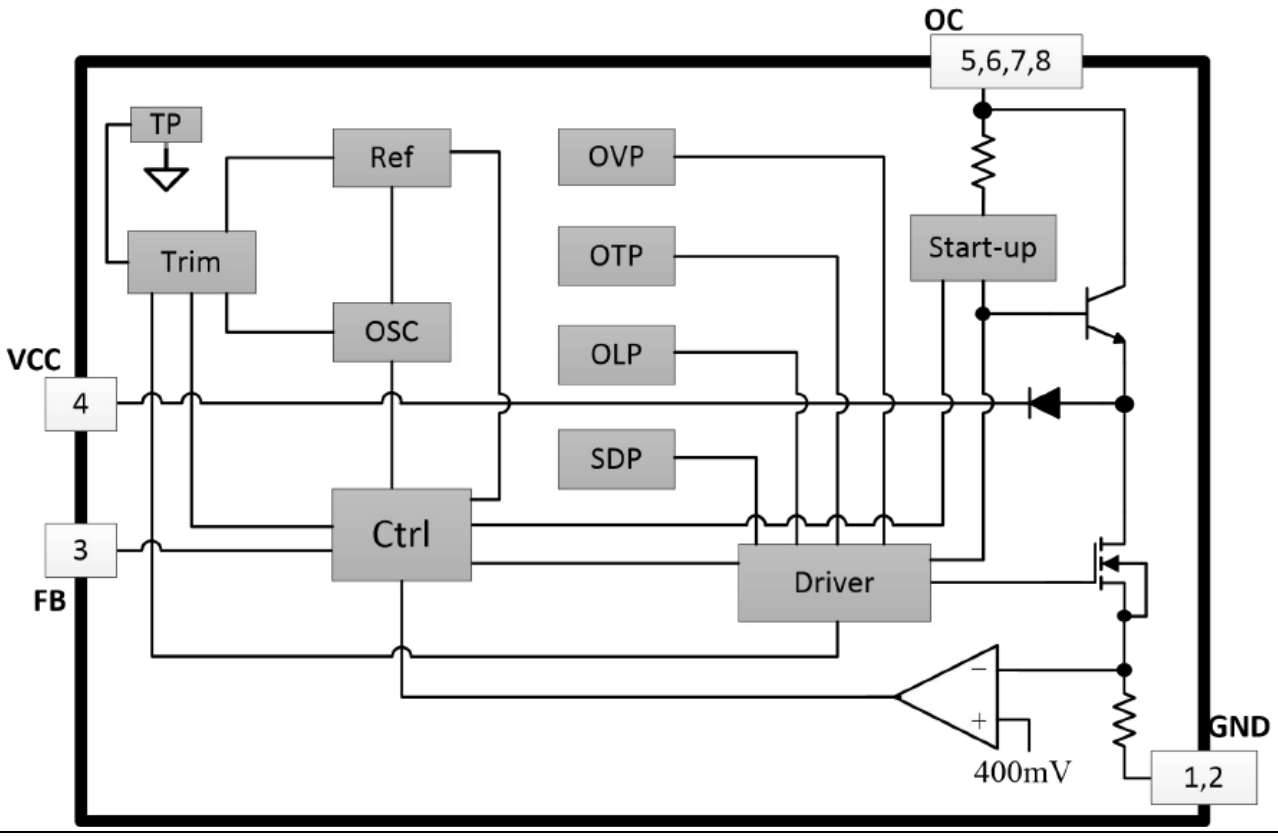

## Description

A250BDM is a high-performance, low-power PWM control chip with a built-in 700V high-voltage power MOSFET, suitable for power solutions up to 24W. The IC has built-in self-powered circuit, and there are very few peripheral components. The transformer design is simple.

**Table 1. PIN FUNCTION**

| PIN | Symbol | Description |
|---|---|---|
| 1 | GND | Ground |
| 2 | GND | Ground |
| 3 | FB | Feedback Input, connect 1 ~ 4.7nF capacitor to GND |
| 4 | Vcc | Power Supply, connect 47 ~ 100uF capacitor to GND (low ESR) |
| 5,6,7,8 | OC | MOSFET Drain |

## Functional Block Diagram



# Absolute Maximum Ratings

**Table 2.**

| Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|
| $V_{Drain-max}$ | | | 700 | V |
| $I_{peak}$ | | | 1500 | mA |
| $V_{CC}$ | -0.3 | | 8 | V |
| $I_{CC}$ | | 100 | | mA |
| $V_{FB}$ | -0.3 | | 8 | V |
| $V_{CS}$ | -0.3 | | 8 | V |
| $T_R$ | -25 | | 125 | °C |
| $T_{STG}$ | -45 | | 155 | °C |
| $T_W$ | | 280/5s | | °C |

**Table 3. Electrical characteristics**

| Symbol | Description | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{cc(no)}$ | Operating voltage | AC Input: 85V-265V | 4.9 | 5 | 5.9 | V |
| $V_{cc(start)}$ | Startup voltage | AC Input: 85V-265V | | 5.2 | | V |
| $V_{cc(reset)}$ | Restart voltage | AC Input: 85V-265V | 3.3 | 3.6 | 3.9 | V |
| $V_{cc(ovp)}$ | Protection voltage | AC Input: 85V-265V | | 6.1 | | V |
| $I_{vcc(no)}$ | Operating current | Vcc=5V, FB=1.5V | | | 50 | mA |
| $I_{OC(start)}$ | High voltage starting current | AC Input: 85V-265V | 0.3 | 0.6 | 1.2 | mA |
| $t_{(start)}$ | Start-up time | AC Input: 85V | | | 500 | ms |
| $V_{OC(bv)}$ | MOSFET withstand voltage | $I_{oc}$=1mA | 700 | | | V |
| $I_{pk(ocp)}$ | Peak current protection | $V_{CC}$=5V, FB=1.5V-2.8V | 1200 | 1300 | 1400 | mA |
| $F_{SW}$ | Switching frequency | $V_{CC}$=5V, FB=1.5V-2.5V | 61 | 65 | 69 | KHz |
| $F_{SW(GM)}$ | Green Mode Frequency | $V_{CC}$=5V, FB=2.5V-2.8V | 20 | 22 | 24 | KHz |
| $F_{step}$ | Stepped frequency | | | 0.5 | | KHz |
| $V_{FB(olp)}$ | Short circuit protection threshold | | | 0.8 | | V |
| $V_{FB(sfpm)}$ | Frequency conversion threshold | | | 2 | | V |
| $V_{FB(std)}$ | Burst mode threshold | | | 4.2 | | V |
| $T_{SD}$ | Junction temperature | | 120 | 130 | 140 | ℃ |
| $t_{(leb)}$ | Leading edge blanking time | $V_{CC}$=5V, FB=1.5V-2.5V | | 250 | | ns |
| $t_{on(min)}$ | Minimum turn-on time | $V_{CC}$=5V, FB=2.6V | | 500 | | ns |
| $D_{on}$ | Duty cycle of PWM | $V_{CC}$=5V, FB=1.5V-2.5V | 5 | | 70 | % |
| $P_{in(std)}$ | Standby power consumption | AC Input: 265V, unload | | | 270 | mW |

# Description

The A250BDM is a high-performance, low-consumption switching power supply control chip suitable for power supply solutions within 24W. It has built-in functions such as frequency-hopping and frequency dithering function, which can effectively reduce standby power consumption, improve the EMI performance of the system, and meet the EU's sixth-level energy efficiency standard.

## 1. Startup

During power-on, the external VCC capacitor is charged by the internal high-voltage constant current source connected between the OC and VCC pins. When the VCC voltage reaches 5.2V, the startup sequence completes and the circuit enters normal operation mode with PWM output.

## 2. Soft Startup

Upon power-up, the IC initiates PWM pulse output. To prevent instantaneous output voltage overshoot, transformer core saturation, and excessive stress on power switches and secondary rectifiers, the chip integrates a soft-start circuit with the following characteristics:

a. First 128 PWM cycles:

- Primary peak current: 0.5 × $I_{p\_max}$
- Switching frequency: 22 kHz (fixed)

b. 128th to 256th PWM cycles:

- Primary peak current: $I_{p\_max}$ (full scale)
- Switching frequency: 22 kHz (maintained)

c. Beyond 256 PWM cycles:

- Switching frequency increases to 66 kHz

## 3. Feedback Control

The IC employs cycle-by-cycle peak current limiting PWM control, which adjusts the current limit by monitoring the FB feedback voltage.

Operation sequence:

a. When PWM turns on:

- IC monitors power switch output current
- Turns off power switch when current reaches the preset limit
- Waits for next PWM cycle

b. FB voltage regulation (1.2V~2.1V range):

- Current limit varies linearly with FB voltage
- 1.2V: Maximum current limit
- 2.1V: Intermediate current limit

c. Light load operation:

a) FB 2.1V→3V:

- Current fixed at intermediate level
- Frequency decreases linearly from 66kHz to 22kHz

b) FB 3V→3.9V:

- Frequency fixed at 22kHz
- Current decreases linearly to minimum level

d. Load variation response:

- Increasing load: FB voltage decreases
- Decreasing load: FB voltage increases

e. Protection mode:

- Short-circuit/overload protection triggers when FB < 0.8V

## 4. Burst mode (Intermittent operation mode)

Under no-load or light-load conditions:

1. When FB voltage rises above (VDD-0.8)V:
   - The IC stops PWM output
   - Enters low-power standby mode
2. When output voltage slightly drops causing FB < (VDD-0.8)V:
   - The IC resumes PWM pulse bursts
   - Delivers energy to maintain regulated output

This burst mode operation:

- Reduces effective switching frequency
- Improves light-load efficiency by:
  * Minimizing switching losses
  * Maintaining output regulation
  * Optimizing power consumption

## 5. Self-Powering Technology:

The IC employs patented self-powering technology that:

1. Regulates VCC voltage at approximately 5V to supply the IC's operating current internally
2. Eliminates need auxiliary winding of transformer, simplify transformer design

## 6. Frequency Jittering Circuit

EMI Optimization Design:

The IC integrates a frequency modulation circuit to:

a. Meet EMI compliance requirements

b. Reduce EMI design complexity

c. Minimize system cost

Frequency Modulation Scheme:

- Medium/Heavy Load:
  * Base frequency: 65kHz ±8kHz (16-step modulation)
  * Frequency step: 500Hz
  * Spread spectrum range: 57-73kHz
- Light Load:
  * Fixed frequency: 22kHz
  * No frequency modulation
- Ultra-Light Load:
  * PWM operation suspended
  * Burst mode activation

## 7. Slope Compensation

The A250BDM provides slope compensation, superimposing a voltage sawtooth signal on the sampled current signal. When the chip operates in CCM mode, especially when the duty cycle is greater than 50%, it avoids sub-harmonic oscillations in the loop.

## 8. MOSFET Drive

The A250BDM uses a unique drive technology. If the drive capability is too weak, it will result in high switching losses; if the drive is too strong, EMI problems are likely to occur. The A250BDM uses an optimized totem-pole structure. Through reasonable output drive capability and dead-time, it achieves better EMI characteristics and lower losses.

## 9. Protection Functions

The A250BDM has comprehensive protection functions, including cycle-by-cycle current limiting protection (OCP), overload protection (OLP), over-temperature protection (OTP), $V_{DD}$ over-voltage protection, under-voltage protection (UVLO), and output Schottky abnormal protection.

The A250BDM has a built-in line-voltage compensation function for the current-limiting point, which can ensure that the current-limiting point remains constant within the full operating voltage range 85-265VAC of circuit, thus ensuring constant power output.

When an overload or short-circuit occurs, the FB voltage will exceed $\mathbf{V_{TH\_PL}}$. When the $V_{DD}$ is lower than $\mathbf{V_{uvlo(ON)}}$, the chip's overload protection circuit starts to work. The chip turns off MOSFET. After a delay of $T_{stop}$, it enters the $V_{DD}$ restart, after the restart is completed, the circuit can resume normal operation.

After the circuit starts, the auxiliary winding of transformer provides energy to the $V_{DD}$ capacitor. When the VDD voltage exceeds $V_{ovp,}$ the over-voltage protection circuit works. The chip turns off MOFET. After a delay of $T_{stop}$, it enters the $V_{DD}$ restart. After the restart is completed, the circuit can resume normal operation.

When the FB voltage is lower than $\mathbf{V_{TH\_PL}}$ and the $V_{DD}$ voltage drops below $U_{VLO}$, the under-voltage lockout ($U_{VLO}$) circuit of chip turns off the chip. After the $V_{DD}$ restart is completed, the circuit can resume normal operation.

## 10. Over Reflected Voltage Protection

1. Fault Condition:

- Secondary circuit open-circuit fault occurs
- Input bus voltage rises abnormally
- Power transistor OC pin experiences high voltage spikes

2. Protection Trigger:

- When reflected voltage exceeds $V_{OR(ovp)}$ threshold:
  * IC activates reflected voltage overvoltage protection
  * Safeguards power transistor from damage

3. Threshold Calculation:

$V_{OR(ovp)} = Lp \times (Ip/6)$

Where:

- Lp: Primary inductance (μH)
- Ip: Fixed at 1.25A (constant current)
- Resultant VOROVP in microseconds (μs)

## 11. Constant Power Control

To avoid too high power output when high input voltage, there is internal power compensation circuit to keep

the stability of output in both low voltage and high voltage input.

## 12. Design Key Points

1. Power Device Thermal Management:

- Primary heat source: Power switch connected to Pin C
- PCB layout requirements:
  * Expand copper area for Pin C with tin plating
  * Maintain adequate spacing from heat-generating components (e.g. transformers)
  * Minimize thermal coupling effects
- EMI/EMC considerations:
  * Isolate AC signal section from input circuitry
  * Reduce electromagnetic/capacitive coupling

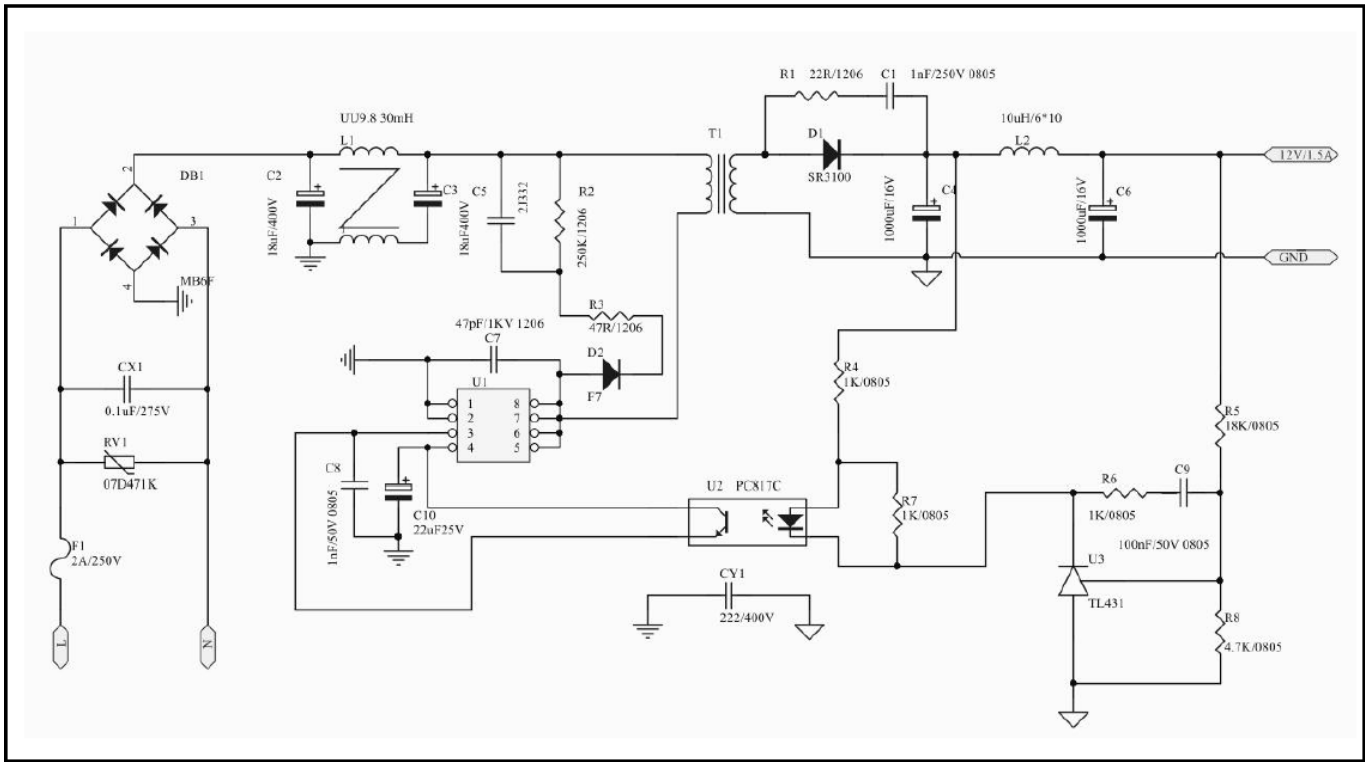
2. High Voltage Protection (OC Pin):

- Withstands >600V potential
- Minimum clearance:
  * 1.5mm from low-voltage circuits
  * Prevents dielectric breakdown/arcing

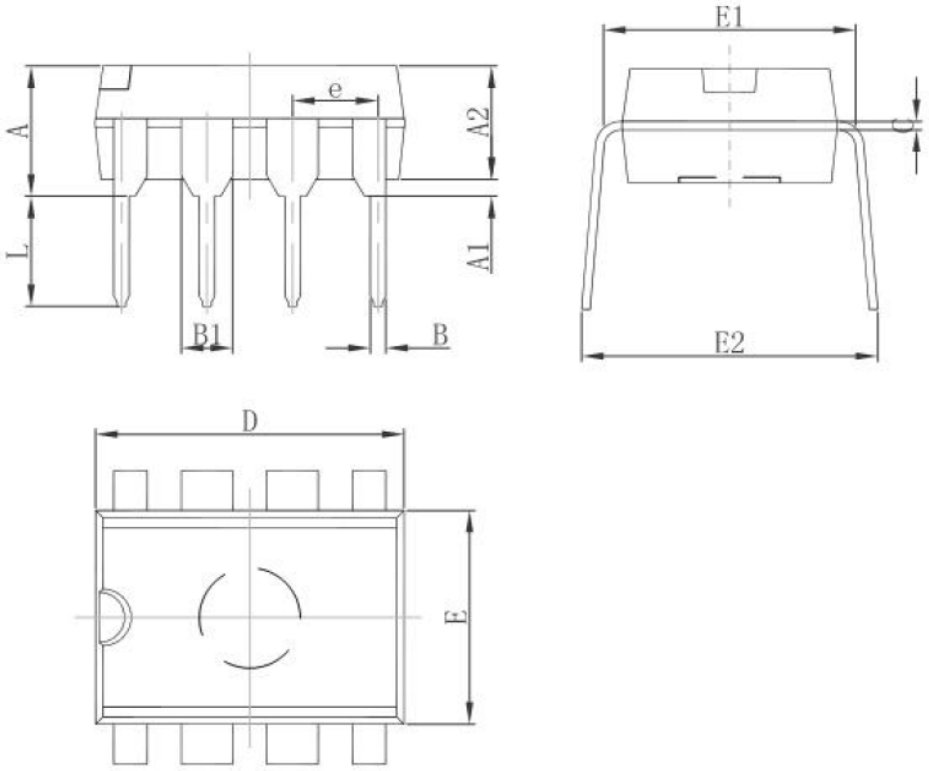
3. Transformer Leakage Inductance Control:

- Inherent non-ideal characteristic requiring mitigation
- Design targets:
  * <5% of primary inductance
- Improvement methods:
  * Sandwich winding technique
  * Interleaved winding configuration
  * Precise bobbin gap control

## 13. Typical Application Circuit Diagram

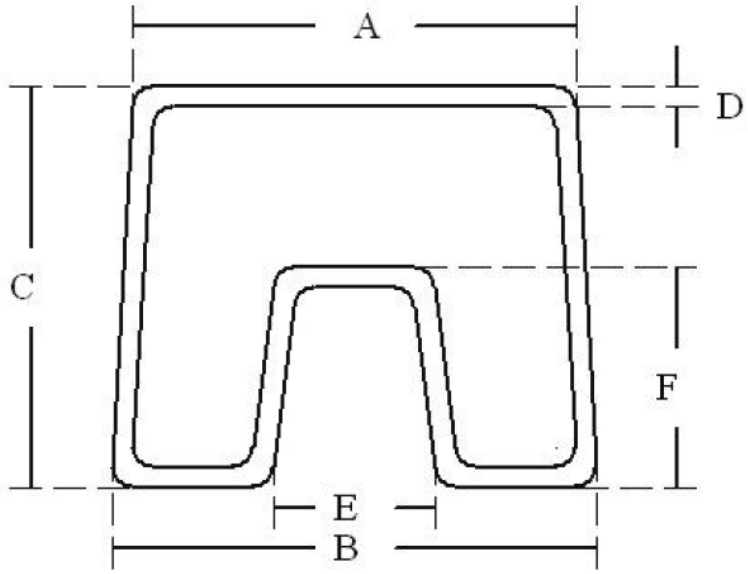


## 14. DIP-8 PACKAGE OUTLINE DIMENSIONS




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 3.710 | 4.310 | 0.146 | 0.170 |
| A1 | 0.510 | | 0.020 | |
| A2 | 3.200 | 3.600 | 0.126 | 0.142 |
| B | 0.380 | 0.570 | 0.015 | 0.022 |
| B1 | 1.524(BSC) | | 0.060(BSC) | |
| C | 0.204 | 0.360 | 0.008 | 0.014 |
| D | 9.000 | 9.400 | 0.354 | 0.370 |
| E | 6.200 | 6.600 | 0.244 | 0.260 |
| E1 | 7.320 | 7.920 | 0.288 | 0.312 |
| e | 2.540(BSC) | | 0.100(BSC) | |
| L | 3.000 | 3.600 | 0.118 | 0.142 |
| E2 | 8.400 | 9.200 | 0.331 | 0.354 |

## 15. Tube Package




| Symbol | Dimensions In Milimeters | | |
|---|---|---|---|
| | Min | Rated Value | Max |
| A | 11.00 | 11.50 | 12.00 |
| B | 11.50 | 12.00 | 12.50 |
| C | 10.00 | 10.50 | 11.00 |
| D | 0.40 | 0.50 | 0.60 |
| E | 3.50 | 4.00 | 4.50 |
| F | 5.00 | 5.50 | 5.10 |

| QTY/tube | QTY/inner carton | QTY/master carton |
|---|---|---|
| 50 | 2000 | 20000 |

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