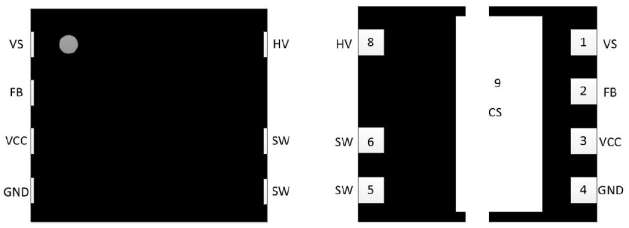
Features



- Wide Voltage Input 85-265V_{AC}
- Switching frequency 250kHz
- Built-in 700V GaN HEMT
- Quasi-Resonant Mode
- Built-in Demagnetization Detection Circuit
- Low standby consumption <50mW@230V_{AC}
- Rich protection: OLP,OCP,OTP,UVLO
- Power capability ⩽45W

Description

A224APG is a quasi-resonant flyback controller AC-DC power switching IC with a monolithically integrated 700V GaN HEMT. The device monitors the drain voltage (V_D) of the power switch and activates the power switch when V_D reaches its valley point, thereby minimizing switching losses and improving electromagnetic interference (EMI) performance.

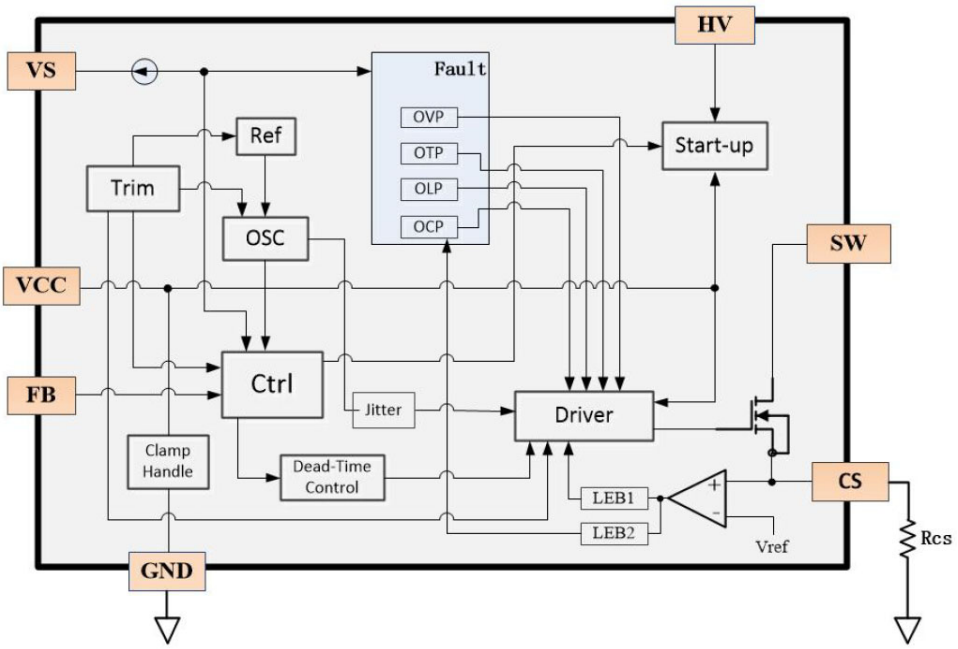
A224APG significantly streamlines the design and manufacturing of flyback AC-DC converters, particularly for applications demanding high conversion efficiency and high-power density.

Rich protection: OVP,OCP,OTP,OLP, UVLO/OVLO.

Table 1. PIN FUNCTION

PIN	Symbol	Description
1	VS	Auxiliary Winding Voltage Sensing Pin
2	FB	Feedback Input
3	VCC	Supply Voltage; Vcc>18V Turn-On,Vcc<5.5V Turn-OFF
4	GND	Ground, connect to primary ground
5,6	SW	GaN HEMT Drain
7	NULL	
8	HV	High-Voltage Start-up PIN
9	CS	Current Sense

Functional Block Diagram



Absolute Maximum Ratings

Table 2.

Symbol	Minimum	Typical	Maximum	Unit
$V_{Drain-max}$		700		V
I_D			5	A
$I_{D-pulse}$ @25°C			9	A
$I_{D-pulse}$ @125°C			5	A
V_{cc}	-0.3		30	V
I_{cc}		1.3		mA
V_{FB}			8	V
V_{CS}			8	V
VS			8	V
P_D			3	W
T_{STG}	-40		150	°C
T_J		150		°C
T_W		260/10s		°C

Table 3. Electrical characteristics

Symbol	Description	Condition	Value			Unit
			Min.	Typ.	Max.	
Vcc						
$V_{CC(start)}$	Start-up Voltage	AC Input: 85V-265V	16.6	18	19.4	V
I_{start}	Start-up Current	V_{cc}=0V	1.5	2.0	2.6	mA
$V_{CC(reset)}$	Rest Voltage		5.1	5.6	6.1	V
$V_{CC(ON)}$	Operating Voltage		7.5	12	26.5	V
$I_{CC\ (ON)}$	Operating Current	V_{cc}=10V	0.8	1	1.2	mA
$V_{CC(OVP)}$	V_{cc} OVP		26.5	28	29.5	V
$I_{SW(OFF)}$	Start-up Circuit Off-state Leakage Current	V_{SW}=600V	48.7	53	57.3	uA
Brown-In / Brown-Out						
V_{Brown_in}	Brown-In Voltage			112		V
V_{Brown_out}	Brown-Out Voltage			90		V
I_{Brown_in}	Brown-In Current		110	125	140	uA
I_{Brown_out}	Brown-Out Current		89	101	113	uA
FB						
$V_{FB(open)}$	Voltage at FB Pin under Open-Circuit Conditions		4.95	5.13	5.35	V
$I_{FB(short)}$	Current at FB Pin connect to GND	FB PIN connect to GND	167	183	204	uA
$V_{FB(vf)}$	Voltage at FB Pin under Frequency Conversion Starting Point		1.4	1.6	1.8	V
$V_{FB(std)}$	Voltage at FB Pin under Standby		0.6	0.7	0.8	V
CS						
V_{ILIM1}	CS PIN Voltage at Peak Current		598	650	702	mV

$V_{CS(min)}$	CS PIN Voltage at Minimum Current		138	150	162	mV
T_{LEB}	Leading Edge Blanking Time	VCS≤960mV	250	300	350	ns
VS Demagnetization Detection						
V_{TH_VS}	Demagnetization Threshold Voltage		27	30	33	mV
V_{VS_OVP}	VS Threshold Voltage		3.3	3.6	3.9	V
Time Domain						
$t_{ON(max)}$	Maximum On-Time		13.8	15	16.2	us
$T_{sw(max)}$	Maximum Switching Period		36.8	40	43.2	us
Protection						
t_{opp}	Overload Protection Restart Time		1840	2000	2160	ms
t_{short}	Short-circuit Protection Restart Time		1840	2000	2160	ms
t_{osd}	Output Short-Circuit Detection Time		386	420	454	ns
T_{SD}	Maximum Protection Temperature		130		150	°C
$R_{DS(on)}$	Power Switch On-Resistance			365	480	mΩ

Feature

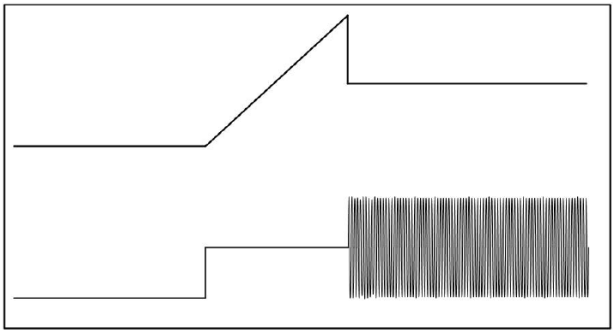
A224APG is a current-mode controlled quasi-resonant flyback AC-DC power management switching IC. It integrates a 700V GaN HEMT, control circuit, and driver circuit, significantly reducing the number of external components required while effectively lowering overall system costs.

A224APG operates in Discontinuous Conduction Mode (DCM). When the transformer's core energy is fully depleted and the primary inductance resonates with the GaN HEMT's junction capacitance to reach their minimum values, the primary power switch is activated. This innovative switching methodology minimizes switching losses and optimizes conversion efficiency across the entire load range.

1. Startup

During power-up, the IC charges the external V_{CC} storage capacitor via an high-voltage start-up circuit to charge the capacitor of Vcc. Once the V_{CC} voltage reaches the start-up threshold ($V_{CC(START)}$), the high-voltage circuit is disabled, completing the start-up sequence.

Under light-load or no-load conditions, the controller operates at its minimum switching frequency. The V_{CC} pin capacitor must be sufficiently large to ensure the V_{CC} voltage remains above the UVLO reset threshold ($V_{CC(RESET)}$) during low-frequency operation.



2. Power-up, Brown-In detection

During power-up, if the input voltage exceeds the Brown-In threshold (V_{Brown_in}) for 3 consecutive PWM cycles, the bus voltage is validated, triggering the soft-start sequence. If validation fails for 6 consecutive PWM cycles, PWM output is disabled. The system initiates a 16ms reset delay, followed by a full restart. Once V_{CC} reaches the start-up voltage ($V_{CC(start)}$), the input voltage detection loop reinitializes.

3. Soft Start-up

Upon successful Brown-In detection, the IC initiates soft-start operation. To prevent output voltage overshoot, transformer core saturation, and excessive stress on the power switch and secondary rectifier during startup, the device integrates an internal soft-start circuit.

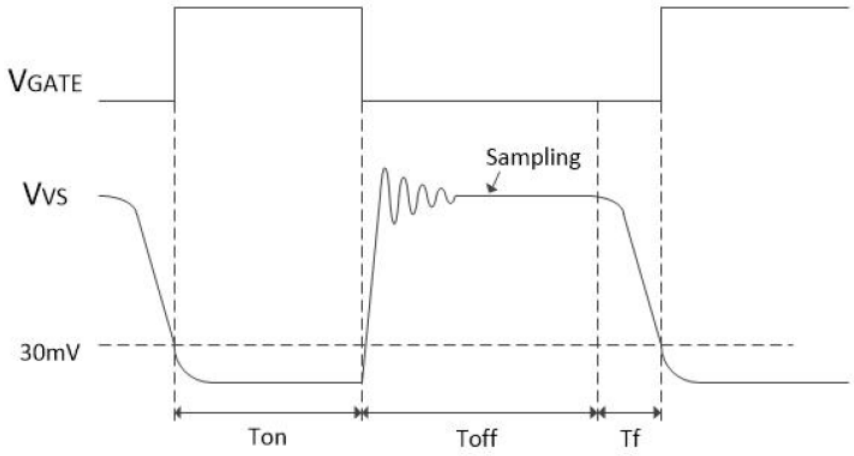
4. During Operation, Brown-Out Detection

During operation, if the input voltage remains below $V_{Brown-out}$ for 32ms, the IC confirms a Brown-Out event, immediately halts PWM output. After a 16ms reset delay, the system reboots: V_{CC} charges to the start-up threshold ($V_{CC(start)}$) and re-enters the Brown-In detection phase.

5. Demagnetization Detection

The IC detects transformer demagnetization by monitoring the VS pin voltage (sampled from the auxiliary winding) to enable valley switching. Once the inductor's stored energy is fully released, the VS voltage begins to decay. When VS falls below a predetermined threshold, the controller activates the power switch via an internal comparator-driven gate driver, initiating the next switching cycle.

The power switch is deactivated when the sampling resistor R_{cs} voltage reaches V_{ILIM1}. Power switch activation is triggered when the auxiliary winding voltage drops below the demagnetization threshold V_{TH_VS}. The flyback converter initiates valley switching by turning on the power switch at the drain voltage valley (minimum resonant point), reducing switching losses and EMI. As illustrated, the power switch is enabled immediately when the VS pin voltage falls below V_{TH_VS}.



6. Quasi-Resonant Mode

The quasi-resonant (QR) flyback mode operates in discontinuous conduction mode (DCM), where the primary switch is turned on at the valley point of the resonant waveform. This occurs after the transformer's core energy is fully depleted, allowing the primary inductance (Lp) and the switch's junction capacitance (Coss) to resonate to their minimum (valley) voltage, thereby minimizing switching losses.

7. Valley Lock-Out

In Quasi-Resonant (QR) operation, conventional frequency clamping limits maximum switching frequency but

causes controller oscillation between valley switching cycles, leading to audible noise and excessive output ripple. To resolve this during load transients, valley-lock control is implemented to fix switching to a specific resonant valley.

8. Frequency Dithering

To reduce electromagnetic interference (EMI), a frequency dithering circuit is implemented by introducing a low-frequency triangular waveform to the PWM comparator's input. This spreads the peak energy of EMI noise across the spectrum, effectively mitigating conducted and radiated emissions.

9. High and low voltage compensation circuit

To mitigate excessive output power under high-line input conditions caused by power switch turn-off delay, the IC incorporates a line voltage compensation circuit, ensuring consistent maximum output power across varying grid voltages.

10. Overload and Short-Circuit Protection

During overload or output short-circuit conditions, the IC triggers overload/short-circuit protection when the VCS voltage exceeds the maximum threshold and persists for a defined duration.

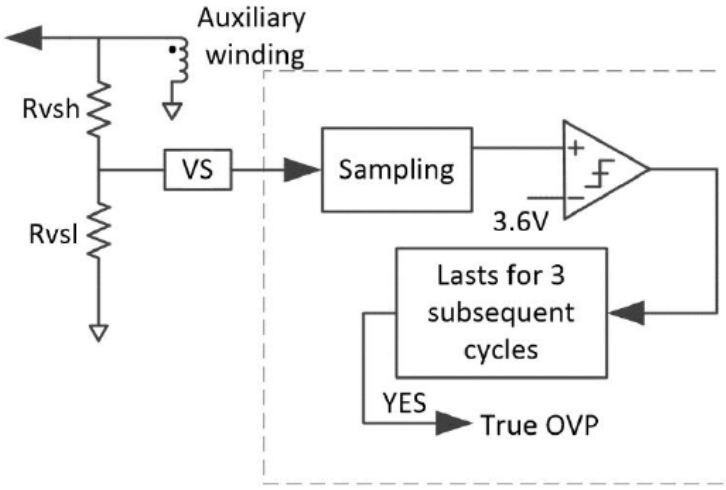
11. Overvoltage protection

The IC accurately monitors the output voltage magnitude via the auxiliary winding's voltage feedback. When an output over-voltage (OV) condition is detected, the primary-side controller immediately disables the PWM output, thereby implementing closed-loop protection.

The output over-voltage protection (OVP) is implemented by monitoring the VS pin voltage during power switch turn-off. This voltage is proportional to the output voltage, with the proportionality determined by the auxiliary-to-secondary winding turns ratio and the auxiliary winding resistive divider ratio. To ensure stable OVP sampling, an internal blanking period filters out leakage inductance spikes that occur at switch turn-off.

When the sampled plateau voltage exceeds the V_{VS_OVP} threshold, an internal counter increments. The converter validates OVP and halts operation after 3 consecutive cycle detections, preventing false triggering.

$$V_{VS} = V_{OUT} * \frac{R_{vsl} * N_A}{(R_{vsh} + R_{vsl}) * N_S}$$



V_{OUT}: Output Voltage N_A: Turns of Auxiliary winding N_s: Turns of secondary winding

12. Leading - Edge Blanking

The transformer's stray capacitance generates a high-current spike during power switch turn-on. The integrated leading-edge blanking (LEB) circuit suppresses this spike to prevent false triggering of the protection circuitry.

13. FB Control

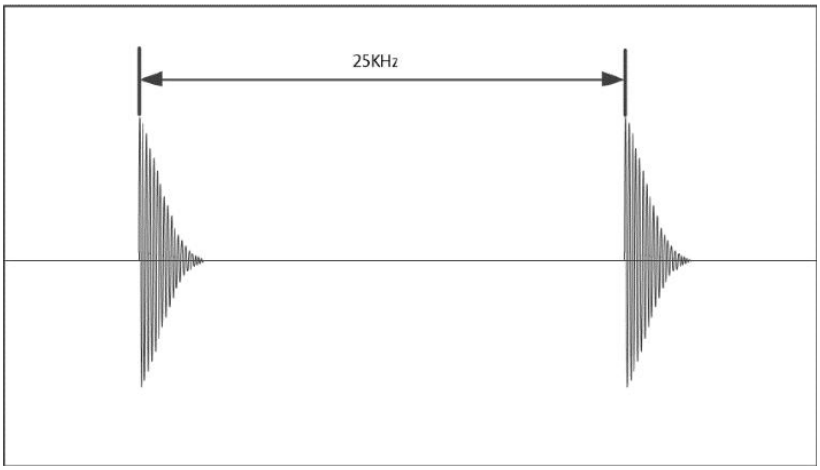
The IC employs a cycle-by-cycle current-limiting PWM control scheme, adjusting the peak current in each switching period based on the FB feedback voltage. When the power switch is turned on, the device monitors the voltage across sense resistor Rcs. Once this voltage reaches the threshold V_{ILIM1}, the power switch is immediately disabled, awaiting the next PWM cycle.

Under varying load conditions, the FB voltage fluctuates within a defined range. The IC utilizes internal hysteresis-based valley-lock processing to ensure stable valley switching. Activating the power switch at the resonant valley minimizes turn-on losses. However, oscillation between adjacent valleys would cause significant frequency variations, leading to audible noise and increased output ripple. Therefore, during steady-state operation, valley switching is strictly locked to a single valley point.

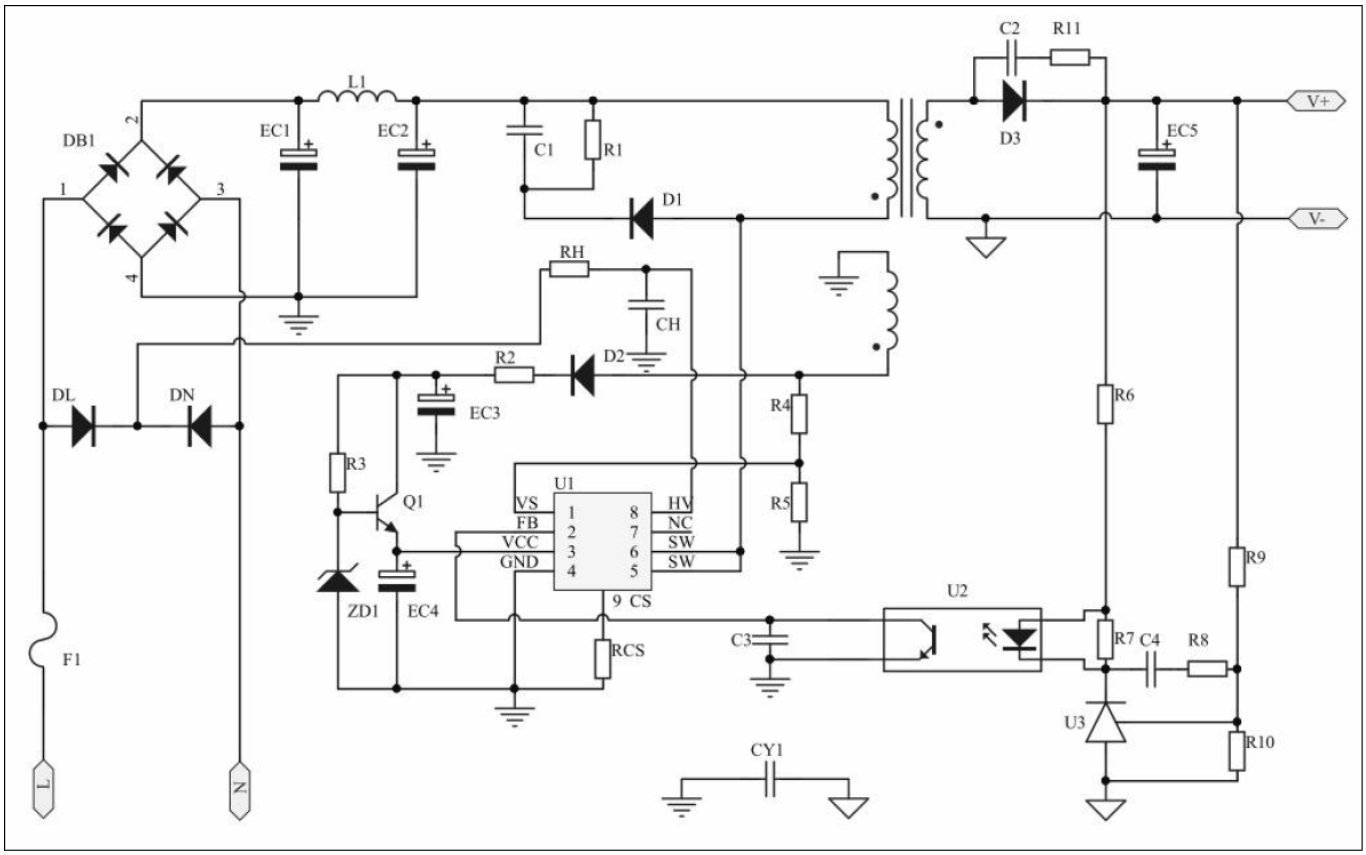
As the load decreases and V_{FB} drops below $V_{FB(vf)}$, the IC progressively reduces the switching frequency (down to a minimum of 25kHz) to maintain efficiency while preventing abrupt current reduction. During the transition from $V_{FB(vf)}$ to $V_{FB(std)}$, the peak current gradually decreases to $V_{CS(MIN)}$/Rcs. If V_{FB} further declines below $V_{FB(std)}$, the IC enters standby mode, halting PWM operation.

Standby exit occurs when V_{FB} exceeds $V_{FB(std)}$ + 50mV, prompting intermittent PWM bursts to regulate output voltage. This burst-mode operation significantly improves light-load efficiency by reducing effective switching frequency.

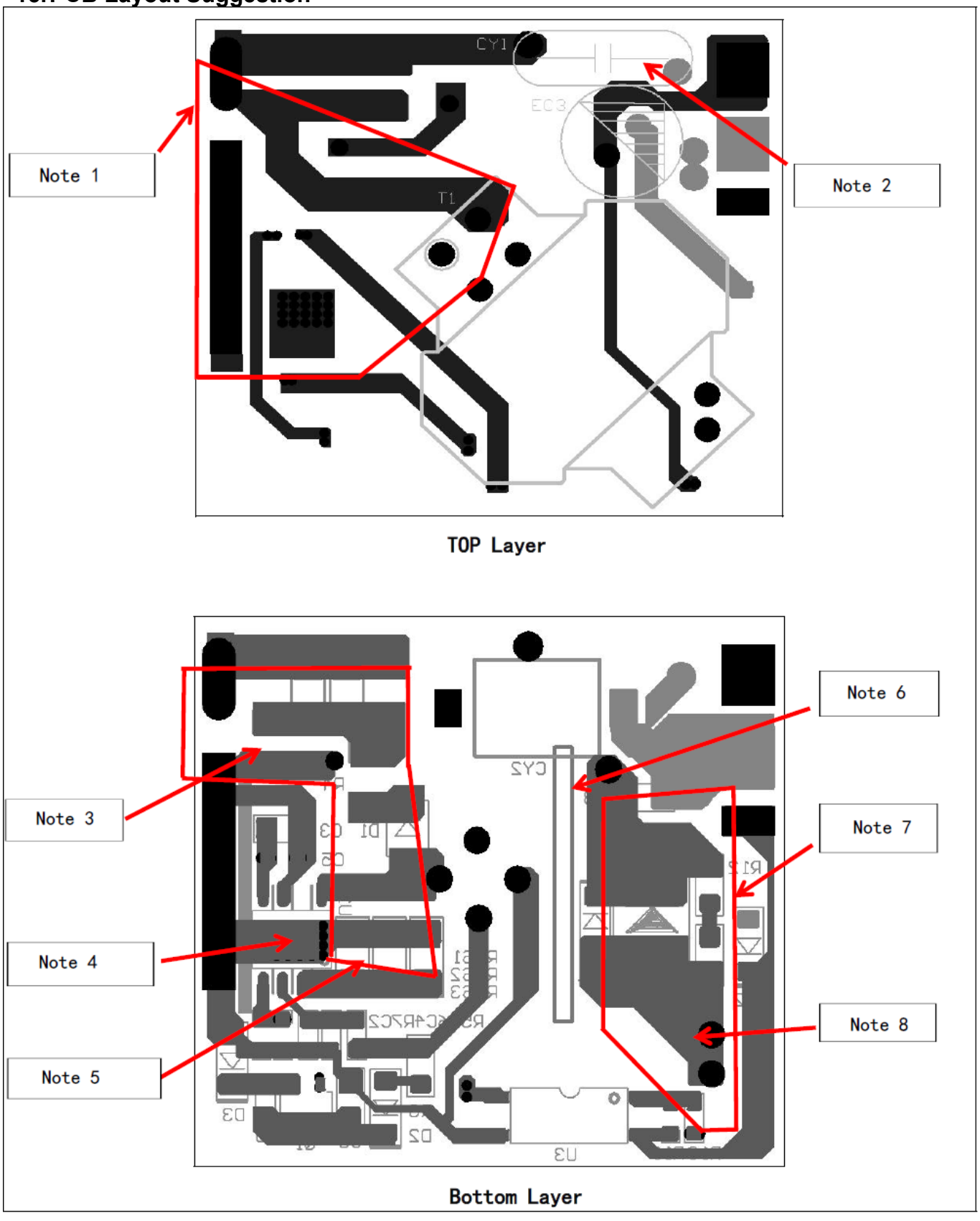
The switching frequency increases progressively from no-load to full-load conditions. To prevent operation within the audible noise spectrum (20Hz-20kHz), the IC implements a minimum frequency clamp at 25kHz, effectively eliminating acoustic noise.



14. Typical Application Circuit Diagram



15. PCB Layout Suggestion



Note 1:

The loop area formed by the input filter capacitor, transformer primary, and the IC's primary-side connections must be minimized to reduce parasitic inductance and suppress high-frequency noise.

Note 2:

The Y capacitor is connected to the primary side to provide surge protection and mitigate common-mode surge currents.

Note 3:

To mitigate EMI, ensure the traces connecting the clamping components, transformer, and IC are minimized in length.

Note 4:

Maximize the CS area to enhance thermal dissipation.

Note 5:

The current sense resistor should be placed close to the IC.

Note 6:

Galvanic isolation between primary and secondary circuits must comply with safety standards.

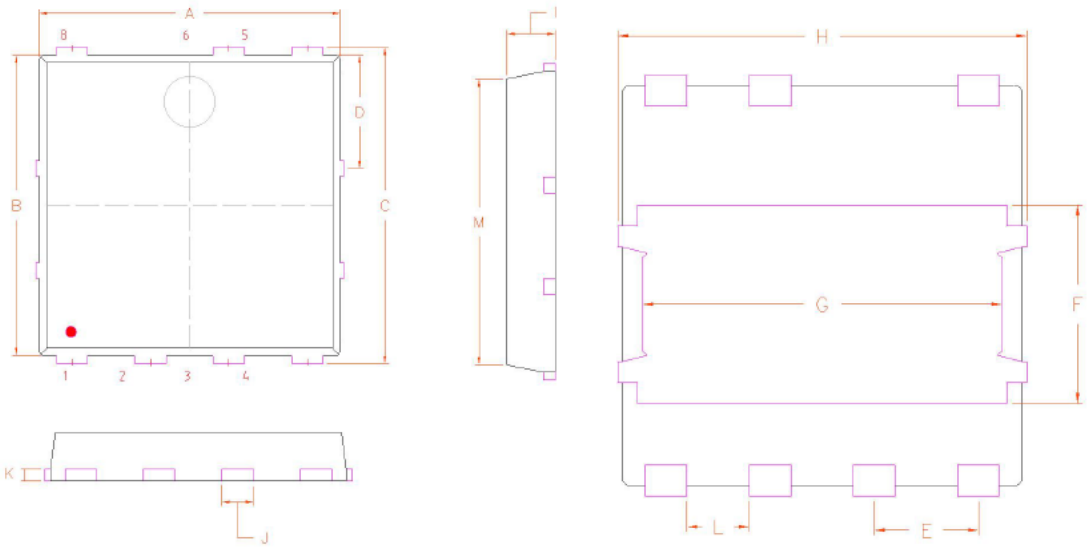
Note 7:

The loop area formed by the secondary-side synchronous rectification (SR) circuit and output filter capacitor must be minimized to reduce parasitic inductance and suppress switching noise.

Note 8:

Maximize the synchronous rectification (SR) pin area to improve thermal dissipation

16. PDFN-8x8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		
	Min	NOM	Max
A	7.60	7.68	7.78
B	7.60	7.68	7.78
C	8.00	8.08	8.18
D		2.90 (NOM)	
E		2.00 BSC	
F		3.80 (NOM)	
G		6.90 (NOM)	
H	7.75	7.85	7.95
I	1.20	1.23	1.30
J		0.80 (NOM)	
K		0.30 (NOM)	
L	1.15	1.20	1.25
M		7.30 (NOM)	

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